Int. J. on Recent Trends in Engineering and Technology, Vol. 8, No. 2, Jan 2013

Low Power Full Adder using 9T Structure

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***Abstract*—In this paper, we propose a new 9T 1-bit full adder. The main objective is full output voltage swing, low power consumption and temperature sustainability. The proposed design is more reliable in terms of power consumption, Power Delay Product (PDP) and temperature sustainability as compared to the existing full adder designs. The design has been implemented 45nm technology on Tanner EDA Tool version 13.0. The simulation results demonstrate the power consumption, delay and power delay product at different input voltages ranging 0.4V to 1.4V.**

***Index Terms*—Full Adder, XOR, XNOR, PDP, Threshold loss.**

I. Introduction

With the continuously increasing demand of laptops, portable personal communication systems and the evolution of shrinking technology, the research effort in low-power micro-electronics has been intensified and low-power VLSI systems have emerged high in demand. Digital integrated circuits commonly use CMOS circuits as building blocks. The continuing decrease in feature size of CMOS circuits and corresponding increase in chip density and operating frequency have made power consumption a major concern in VLSI design.

In recent years, the growing demand for high-speed arithmetic units in CPU (central processing unit), ALU (Arithmetic logic unit), DSP (Digital signal processors) architectures and microprocessors has led to the development of high-speed adders as addition is an obligatory and indispensable function in these units. Adder is the core element of complex arithmetic circuits like addition, subtraction, multiplication, division, exponentiation etc. Thus, enhancing the performance of the full adder block leads to the enhancement of the overall system performance Ref. [1-3]. As a result, design of a high-performance full adder is very useful and important.

Power dissipation has become a prime constraint in high performance applications, especially in portable and battery operated systems so it is necessary to reduce power consumption.

With the development of CMOS technology, the minimum gate length of transistors continues to decrease, and the characteristic frequency also will be rising. With the lowering of threshold voltage in ultra deep submicron technology, lowering the supply voltage appears to be the most eminent means to reduce power consumption. However, lowering supply voltage also increases circuit delay and degrades the drivability of cells designed with certain logic styles Ref. [4].

In CMOS circuits, there are three major source of power consumption Ref. [5] vide

A. Switching Power: Occurs during output transitions due to output switching.

B. Short Circuit Power: The short circuit current between power supply and ground gives short circuit power.

C. Static Power: Caused by leakage current and static current.

Accordingly, the average power consumption in the conventional CMOS digital circuits can be expressed as the sum of these three components (1) Ref. [6]

$$P_{avg} = P_{switching} + P_{short\ circuit} + P_{static} \quad (1)$$

The Power Delay Product (PDP) is a quantitative measure of the efficiency of the tradeoff between average power consumption and speed and is particularly important when low power operation is needed. As its name suggests that, it is the power, delay product. Thus, it can be determined by multiplying the average power consumption and the delay.

The full adder design can be broken into three parts as shown in Fig. 1. Block 1 comprises of either XOR or XNOR circuits. Block 2 and Block 3 comprises of mainly multiplexer also from gates like XOR and XNOR. Block 1 produces intermediate signals X and X' that are passed onto Block 2 and Block 3 that generates Sum and Carry outputs respectively Ref. [7].

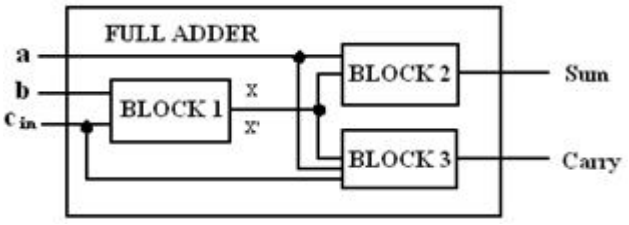

Figure 1. Block diagram of 1-bit Full Adder

The Tanner EDA Tool is used for back-end designing and the S-Edit and T-spice tools for realizing the designed VLSI adders. The S-edit is used for designing of the schematic of a circuit and T-spice is used to observe the output waveform on the W-edit screen.

II. Previous Work

The full adder operation can be stated as follows in (2) and (3). Given the three 1-bit inputs A, B, and C_{in}, it is desired to calculate the two 1-bit outputs Sum and Carry Ref. [8], where

$$Sum = A \oplus B \oplus C_{in} \quad (2)$$

$$Carry = AB + C_{in}(A \oplus B) \quad (3)$$

The circuit shown in Fig. 2 is the schematic of existing 8T full adder Ref. [9]. The sum output was implemented using cascaded 3T XOR gate and Carry output was designed by

DOI: 01.IJRTET.8.2.550

2T multiplexer. This 8T full adder has threshold loss problem due to the simultaneous enabling of NMOS and PMOS transistors as they try to transfer opposite signals on the output result into voltage degradation. There was a major degradation in the output voltage that might lead to functional failure as well as increased power consumption at higher voltages.

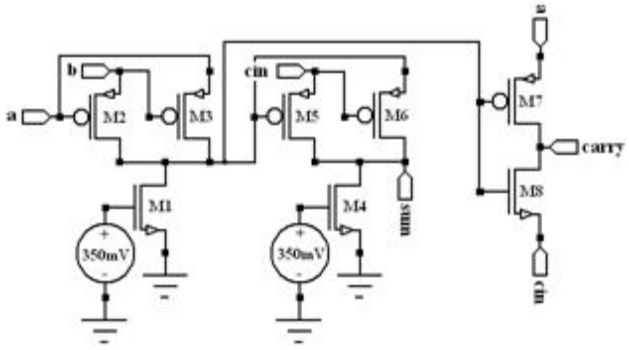

Figure 2. Existing 8T full adder

The Fig. 3 shows the schematic diagram of existing 9T full adder using an extra M9 transistor to improve the performance of 8T full adder Ref. [9]. The Sum output was basically obtained by cascaded three inputs XOR gate in addition to an extra transistor M9. Carry was implemented using 2Tmultiplexer. 8T full adder was confronted with problems for certain input vectors. This problem was eliminated in the design of Fig. 1 by adding an extra transistor M9. Although it has area overhead of one transistor, but still its power consumption was reduced than the 8T adder circuit. This circuit shows nominal improvements in power when compared with adder of Fig. 1, but still had threshold loss.

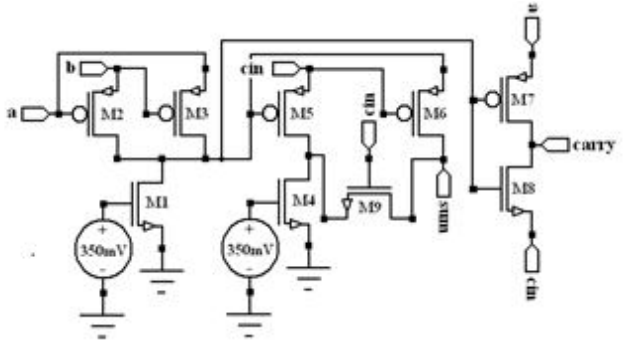

Figure 3. Existing 9T full adder

III. Proposed 9T Full Adder Design

The schematic of proposed 9T full adder cell is shown in Fig. 4 and performance table of the full adder designs in Table I. In this circuit 3T XOR gate and a multiplexer are used to implement Sum and one multiplexer to implement the Carry. The selector circuit of the output multiplexers is output of first stage XOR. The Sum output is "A", when the output of the first stage is "0". When the output of the first stage is "1", then the Sum output depends on the input "A", i.e. if "A=0" the Sum output is same as the output of the first stage, otherwise it is "0". The Carry output also depends on the output of the first stage i.e., "Carry=A", when the output of the first stage is "1", and when the output of the first stage is "0", then "Carry = C_{in}".

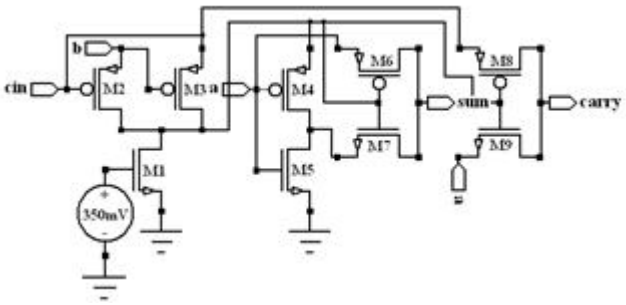

Figure 4. Proposed 9T full adder

Therefore, the operation of Sum and Carry output was based on implementation of XOR operation between the inputs B and C_{in} which is indicated in Table II. and Table III.

Table I. Performance Table Of Full Adder Designs

A	B	C_{in}	Sum (Figure 1)	Sum (Figure 2)	Sum (Figure 3)
0	0	0	0	0	0
0	0	1	**63% of logic "1"**	**85% of logic "1"**	**1**
0	1	0	63% of logic "1"	85% of logic "1"	85% of logic "1"
0	1	1	0	0	0
1	0	0	85% of logic "1"	85% of logic "1"	85% of logic "1"
1	0	1	0	0	0
1	1	0	0	0	0
1	1	1	**85% of logic "1"**	**85% of logic "1"**	**1**

Table II. Conditions For Sum Output

$B \oplus Cin$	A	Sum
0	-	A
1	0	$B \oplus Cin$
1	1	0

Table III. Conditions For Carry Output

$B \oplus Cin$	Carry
0	C_{in}
1	A

The proposed design shows voltage drop for certain input combinations that can be assumed as logic "1", because the voltage drop is very less. Table I shows that the proposed 9T full adder design have better performance compare to the existing full adder designs.

IV. Simulation Results

We have performed simulations using Tanner EDA Tool version 13.0 at 45nm technology with the input voltage ranges from 0.4V to 1.4V in step of 0.2V. In order to prove that the proposed design is consuming low power, have better temperature sustainability and better performance at various input voltages and temperature, simulations are carried out for power consumption and delay and results the PDP.

Fig. 5 shows that the power consumption of the full adder design increases with increase in the input voltage. The proposed design of the full adder has remarkably less power consumption compare to the existing full adder designs.

DOI: 01.IJRTET.8.2.550

Fig. 6 shows that the power consumption of the full adder design increases with increase in the temperature at 0.4V input voltage. The increase in temperature results into increase carrier mobility and due to this, random motion of electrons and holes will increase and hence more number of electron hole pairs will be formed in the interfacial region of the MOSFET, thereby leading to increment in threshold voltage. This increment in the threshold voltage will give rise to the power consumption of the device.

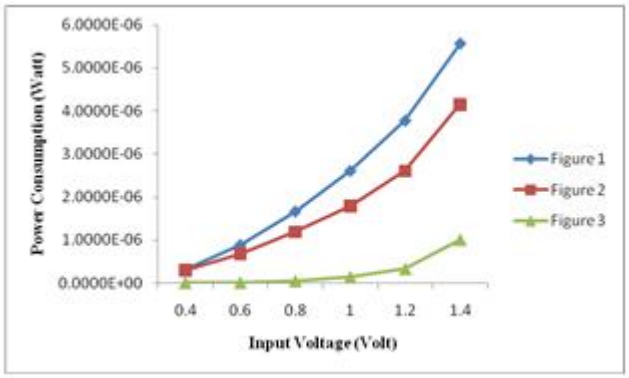

Figure 5. Power Consumption vs Input Voltage

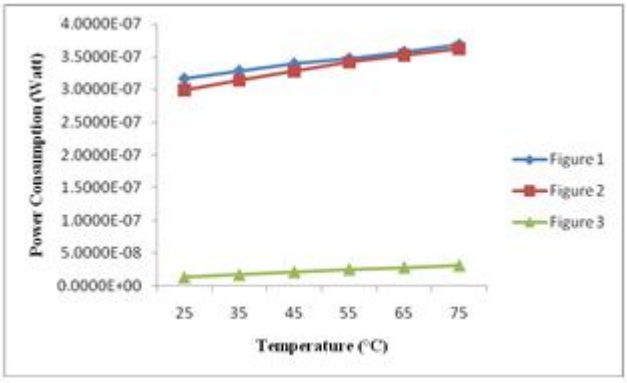

Figure 6. Power Consumption vs varying temperature at 0.4V Input Voltage

From Fig. 7 and Fig. 8 it is evident that the PDP of proposed full adder design better than the existing full adders.

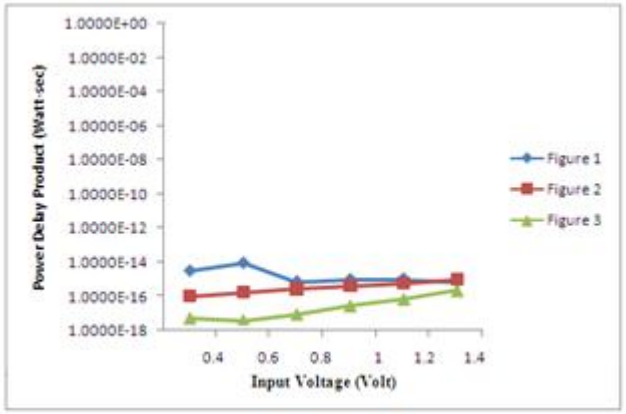

Figure 7. PDP vs Input Voltage

Conclusion

A new 9T full adder design is proposed. According to the simulation results, the proposed design offers a better and more competitive results than other existing designs so it can be operated at low voltage and has better output voltage swing. The proposed 9T full adder design shows 75%, 82% improvement in terms of power consumption and 76%, 69% improvement in terms of PDP in comparison to existing 8T, 9T full adder design respectively. The proposed design is more reliable in terms of power consumption, PDP and temperature sustainability. Thus, the proposed design is a good option for low power applications.

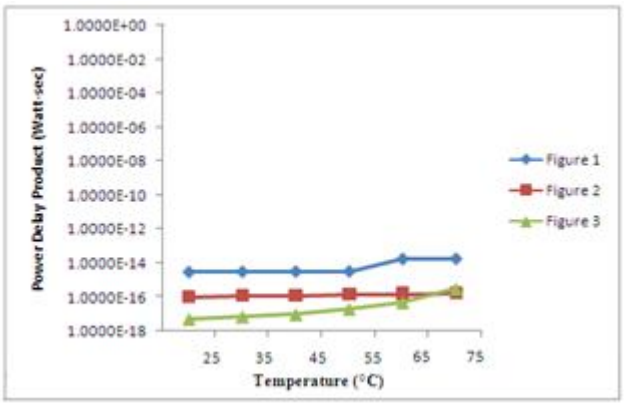

Figure 8. PDP vs varying temperature at 0.4V Input Voltage

Acknowledgment

I am very thankful to MITS (Deemed University) for providing a good laboratory facility. We simulate the result on Tanner EDA Tool version 13.0.

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DOI: 01.IJRTET.8.2.550